ABSTRACT

A method to generate an optimum phase shifted sampling clock for sampling a synchronized video signal A(t) having a synchronization signal SYNC pulse is achieved. The method comprises, first, generating a sampling clock having a first edge aligned with a trailing edge of the SYNC pulse. The sampling clock period comprises the SYNC pulse period divided by M. Second, the number of sampling clock cycles N is counted from the trailing edge of the SYNC pulse until the A(t) value at the first edge of the sampling clock exceeds a minimum value. Third, the sampling clock and the SYNC pulse are phase shifted forward until the A(t) value at the first edge of the sampling clock first exceeds a minimum value on clock cycle N-1 to thereby establish a worst case phase shift of the sampling clock. Finally, A(t) is sampled at an offset from the worst case phase shift to thereby generate an optimum phase shifted sampling clock.